

WHAT IS CLAIMED IS:

1. A synchronization circuit comprising:

a reference pulse;

a first variable delay circuit for generating a first pulse to be synchronized with said reference pulse, a second pulse which is leading in the phase for a certain period to said first pulse, and a third pulse which is delayed in the phase for a certain period from said first pulse;

a first phase comparing circuit for comparing said reference pulse with said first pulse;

a second phase comparing circuit for comparing said reference pulse and said second pulse and said third pulse; and

a control voltage generating circuit for generating a control voltage of said first variable delay circuit by receiving a comparison output of said first phase comparing circuit and a comparison output of said second phase comparing circuit;

wherein said control voltage generating circuit generates the control voltage by giving priority to the comparison output of said second phase comparing circuit with respect to the comparison output of said first phase comparing circuit, and also generates, after said reference pulse and said second pulse or third pulse are matched in the phases with said second phase comparing circuit, said control voltage by the comparison output

of said first phase comparing circuit.

2. The synchronization circuit according to claim 1, wherein said variable delay circuit comprises a plurality of stages of a unit variable delay circuit, wherein said second pulse is an input pulse of said unit delay circuit to form said first pulse, and wherein said third pulse is an output pulse of said unit delay circuit to receive said first pulse.

3. The synchronization circuit according to claim 2, wherein said synchronization circuit is mounted over a semiconductor integrated circuit device,

wherein said synchronization circuit comprises a second variable delay circuit including a plurality of unit delay circuits for forming said first pulse of said first variable delay circuit and being controlled in the delay time thereof with said control voltage,

wherein said reference pulse is inputted from the external terminal of said semiconductor integrated circuit device and then inputted to said first and second variable delay circuits, and

wherein the pulse synchronized with said reference pulse is outputted from said second variable delay circuit.

4. The synchronization circuit according to claim 3,

wherein said reference pulse is inputted to said first and second variable delay circuits via an input

buffer,

wherein an output pulse generated by said second variable delay circuit is outputted from the external terminal via an output buffer, and

wherein a replica circuit having delay time equivalent to that of said input buffer and output buffer is provided between said input buffer and said first variable delay circuit.

5. The synchronization circuit according to claim 4, further comprising;

a frequency dividing circuit for dividing the frequency of said reference pulse;

a frequency dividing/distributing circuit for dividing the frequency of said reference pulse in the dividing ratio which is equivalent to that of said frequency dividing circuit to distributing them to multiphase clocks corresponding to the frequency dividing ratio;

a second variable delay circuit comprising a plurality of stages thereof for respectively delaying the multiphase clocks of said frequency dividing/distributing circuit; and

a waveform combining circuit for generating the pulse corresponding to said reference pulse by receiving a delayed output of said variable delay circuit.

6. A synchronization circuit comprising;

a reference pulse;

a frequency dividing circuit for dividing the

frequency of said reference pulse;

a first variable delay circuit for generating a first pulse to be synchronized with the frequency-divided pulse of said frequency dividing circuit;

a first phase comparing circuit for comparing said frequency-divided pulse with said first pulse;

a frequency dividing/distributing circuit for dividing the frequency of said reference pulse and generating multiphase clocks corresponding to the frequency dividing ratio;

a second variable delay circuit which is configured in the identical structure to said first variable delay circuit and comprises a plurality of stages for respectively delaying the multiphase clocks formed in said frequency dividing/distributing circuit;

a waveform combining circuit for generating the pulse corresponding to said reference pulse by receiving the delayed output from a plurality of stages of said second variable delay circuit; and

a control voltage generating circuit for generating the control voltages of said variable delay circuit and said second variable delay circuit by receiving a comparison output of said first phase comparing circuit.

7. The synchronization circuit according to claim 6, wherein said synchronization circuit is mounted over a semiconductor integrated circuit device,

wherein said reference pulse is inputted from the

external terminal of said semiconductor integrated circuit device and is then inputted to said first and said second variable delay circuits.

8. A synchronization method comprising the steps of:

forming a first pulse to be synchronized with a reference pulse by a first variable delay circuit, a second pulse which is leading in the phase for a certain period to said first pulse and a third pulse which is delayed in the phase for a certain period from said first pulse;

comparing said reference pulse with said first pulse by a first phase comparing circuit;

comparing said reference pulse with said second pulse and said third pulse by a second phase comparing circuit; and

forming a control voltage with a control voltage generating circuit by giving priority to a comparison output of said second phase comparing circuit with respect to a comparison output of said first phase comparing circuit, matching the phase of said reference pulse with the phase of said second pulse or said third pulse, and then matching, after said matching of phases, the phase of said reference pulse with the phase of said first pulse by forming said control voltage from the comparison output of said first phase comparing circuit.

9. A synchronization method comprising the steps of:

dividing the frequency of a reference pulse by a

frequency dividing circuit;

forming a first pulse to be synchronized with the frequency-divided pulse of said frequency dividing circuit by a first variable delay circuit;

comparing said frequency-divided pulse with said first pulse by a first phase comparing circuit;

dividing the frequency of said reference pulse and forming multiphase clocks corresponding to the frequency dividing ratio by a frequency dividing/distributing circuit;

delaying respectively multiphase clocks generated by said frequency dividing/distributing circuit with a plurality of stages of a second variable delay circuit configured in the same structure as said first variable delay circuit,

generating, by a waveform combining circuit, the pulse corresponding to said reference pulse from the delayed output of said second variable delay circuit of a plurality of stages; and

forming, by a control voltage generating circuit, a control voltage of said first and second variable delay circuits corresponding to a comparison output of said first phase comparing circuit.